

Fault Attacks against your Zen

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Based on:

One Glitch to Rule Them All: Fault Injection Attacks Against AMD's Secure Encrypted Virtualization, R. Bühren, H. N. Jacob, T. Krachenfels, J.-P. Seifert, ACM CCS 2021.

Insecure Until Proven Updated: Analyzing AMD SEV's Remote Attestation, R. Bühren, J.-P. Seifert, Christian Werling, ACM CCS 2019.

On authenticated computing and RSA-based authentication, J.-P. Seifert, ACM CCS 2005.



17th September 2021 @ FDTC 2021

Agenda

Amusing history

What is Zen/AMD SEV?

Research question

Glitching the AMD SP

Conclusions

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Do you remember the invited talk?

FDTC 2005

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FDTC 2005

Reviewing and classifying the basics of fault injection attacks

Jean-Pierre Seifert

FDTC 2005

Edinburgh, 2nd September

Systems
Technology Lab

intel

Do you remember the invited talk?

FDTC 2005

On Fault Attacks and Trusted Computing

Jean-Pierre Seifert

FDTC 2005

Edinburgh, 2nd September

Systems
Technology Lab

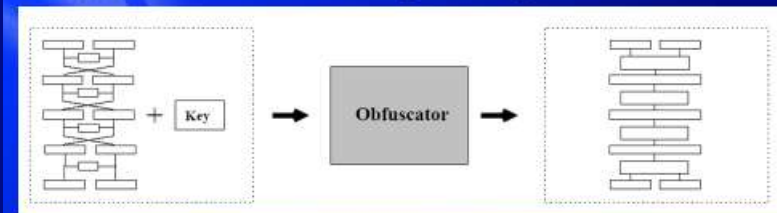
intel

VMs for Fault Injection?

VMM = software that manages the machine's real resource among VMs.

As the VMM has the full control over a VM it is very simple to inject via a VMM from time to time faults into the execution of a cipher.

Application: Very easy way to circumvent sw tamper-resistance enhancing methods like obfuscation - you don't have to do the hard reverse-engineering task:



gy Lab

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Conclusion

It is of great wisdom to have a trustworthy VMM vendor.

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**“THE CLOUD IS
SOMEONE ELSE'S
COMPUTER”**



Alexis Lê-Quốc from New York, United States (https://commons.wikimedia.org/wiki/File:Half_filled_server_racks.jpg), „Half filled server racks“, <https://creativecommons.org/licenses/by-sa/2.0/legalcode>

“THE CLOUD IS
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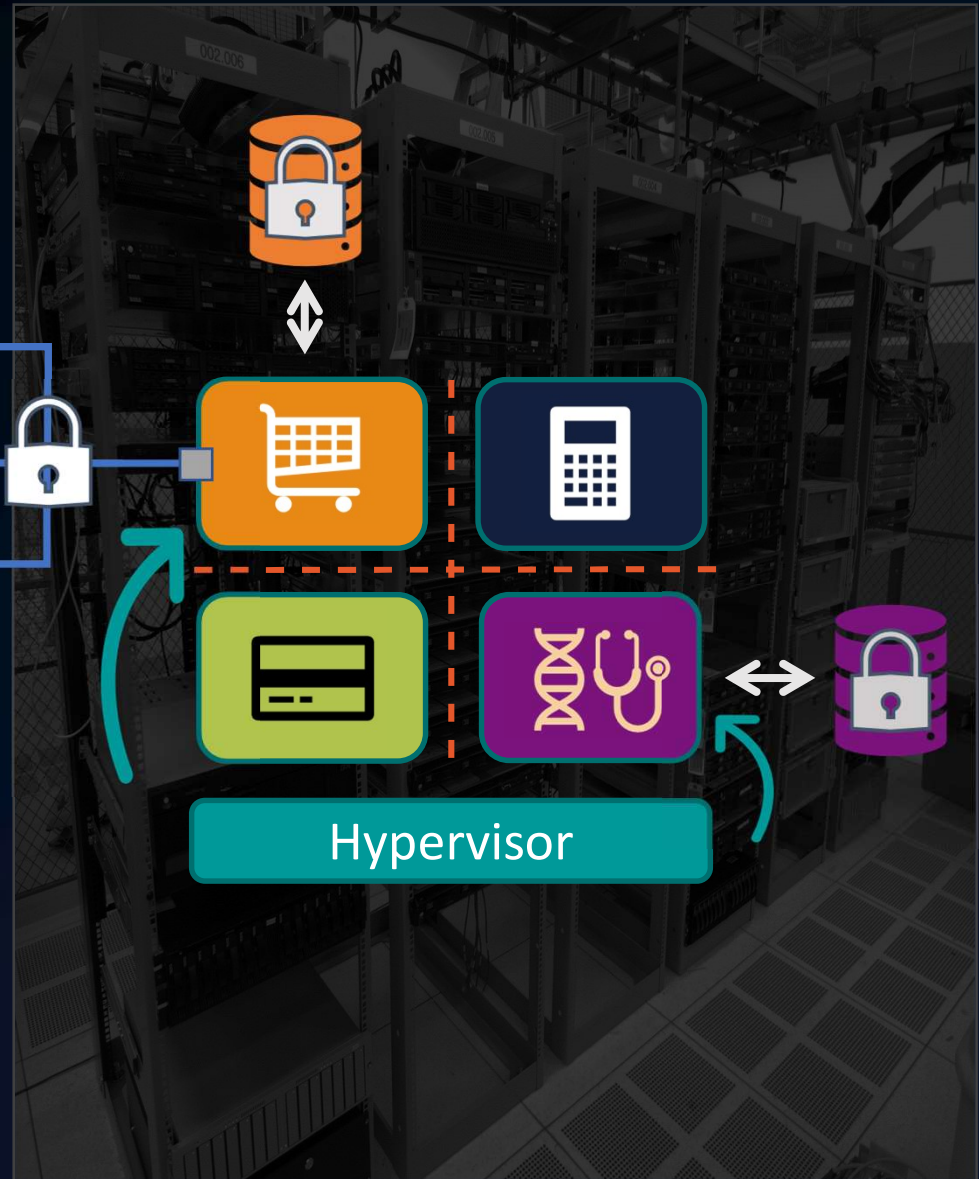
Data-At-Rest: disk encryption

Data-In-Transit: e.g. TLS

Data-In-Use: unprotected



Hypervisor



“... SEV protects data-in-use enabling customer workloads to be protected cryptographically from each other as well as protected from the hosting software.

Even an administrator with malicious intentions at a cloud data center would not be able to access the data in a hosted VM.”

https://developer.amd.com/wordpress/media/2013/12/AMD_Memory_Encryption_Whitepaper_v7-Public.pdf

SECURE ENCRYPTED
VIRTUALIZATION

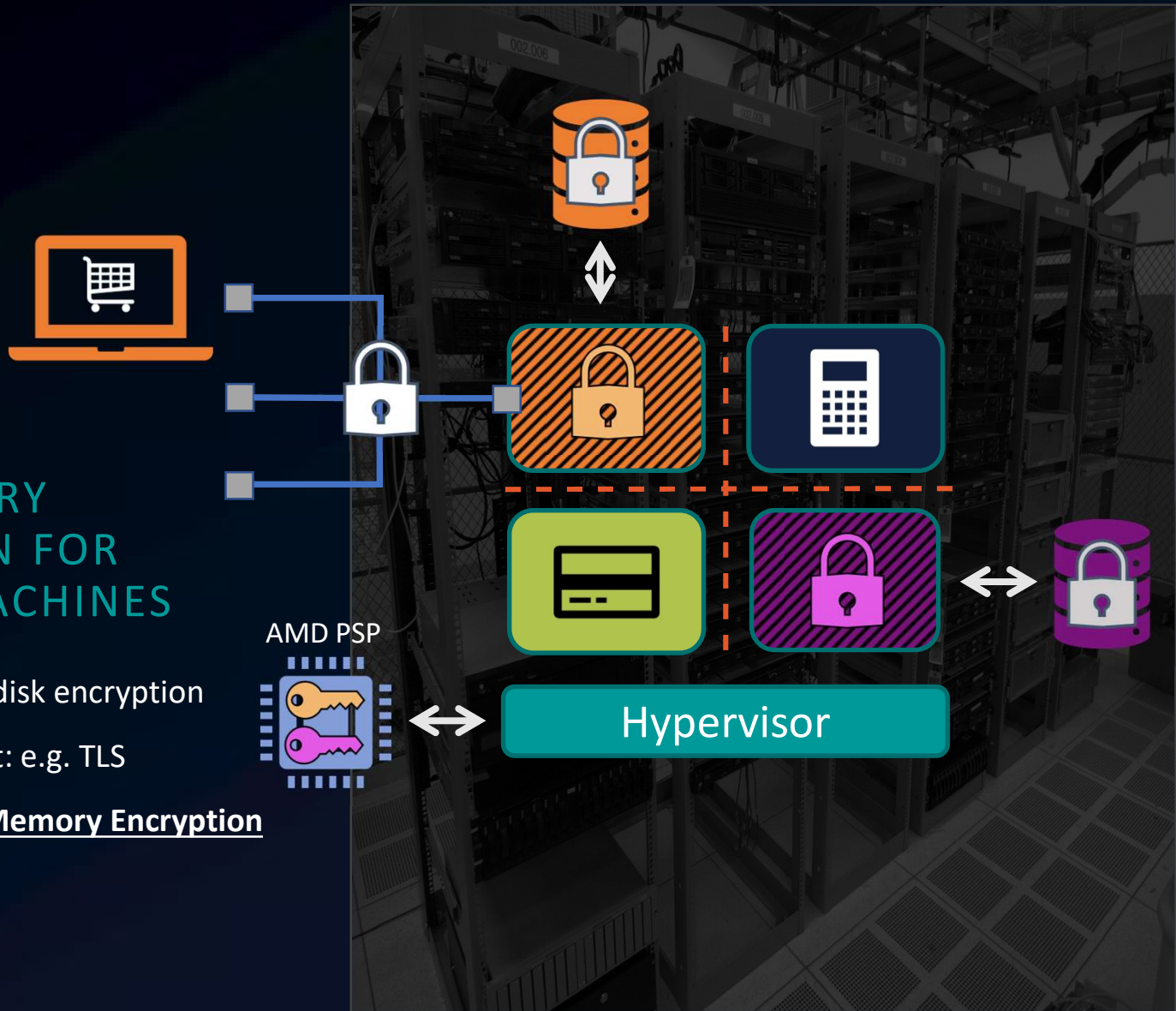
AMD

SEV: MEMORY ENCRYPTION FOR VIRTUAL MACHINES

Data-At-Rest: disk encryption

Data-In-Transit: e.g. TLS

Data-In-Use: Memory Encryption (AES-128)

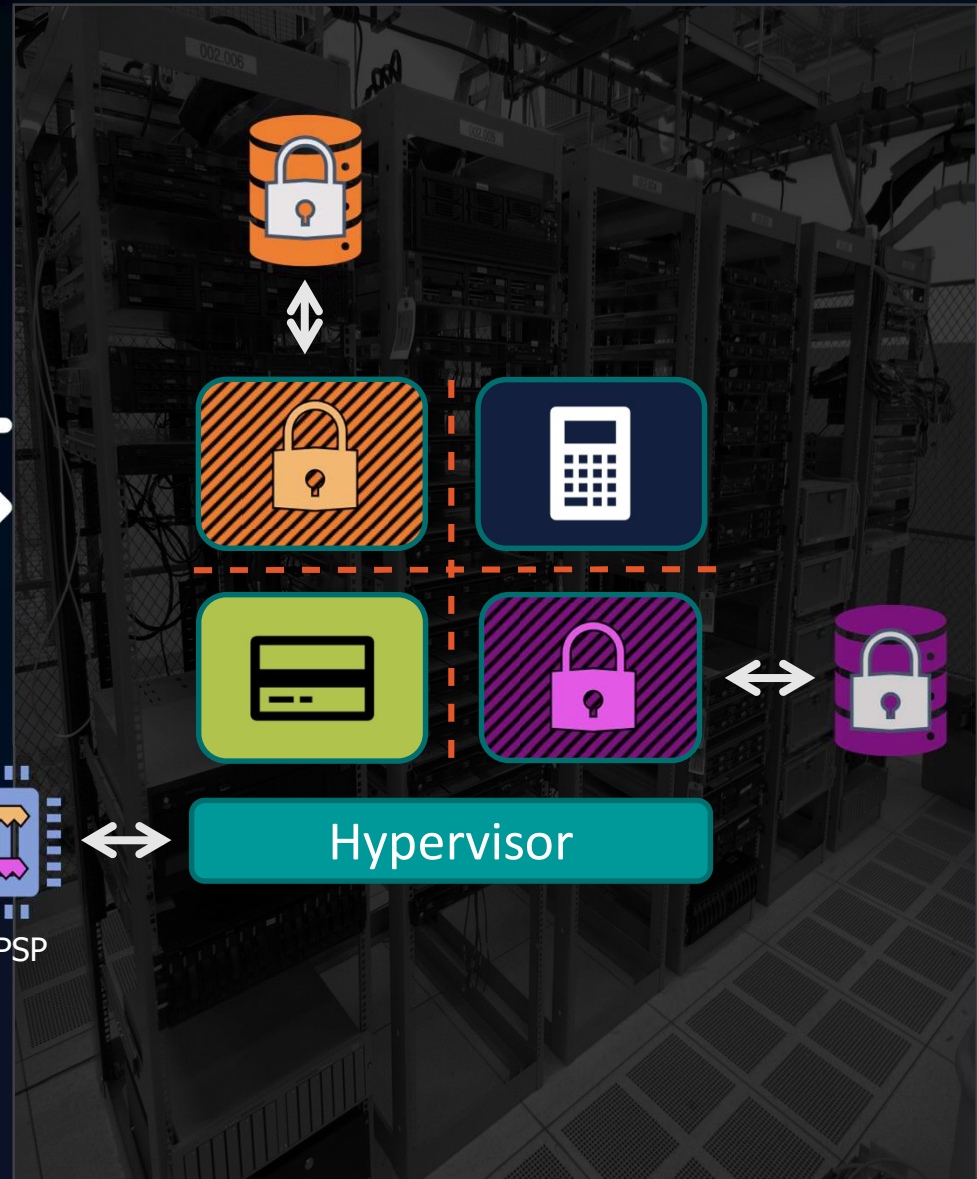
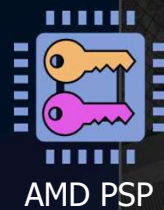
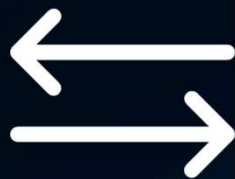




SEV: MEMORY ENCRYPTION FOR VIRTUAL MACHINES

A customer needs to ensure that her virtual machine was deployed with SEV protection in place!

Remote Attestation



SEV Extensions

SEV

- VM memory encryption
- Guest **registers** are NOT encrypted

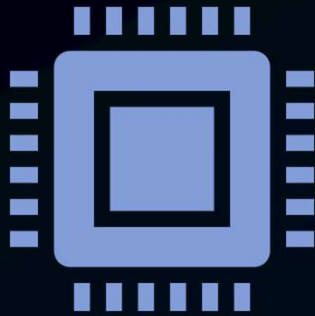
SEV ENCRYPTED STATE

- **register** encryption

SEV SECURE NESTED PAGING

- **software-based** memory integrity protection¹
- Versioned Chip Endorsement Key (VCEK)
- New VM migration mechanism
- VM privilege levels (VMPLs)
- Trusted platform information (CPUID)

¹Fault Attacks on Encrypted General Purpose Compute Platforms, R. Buhren, S. Gueron, J. Nordholz, J.-P. Seifert, J. Vetter, CODASPY 2017: 197-204



SEV: AMD-SP

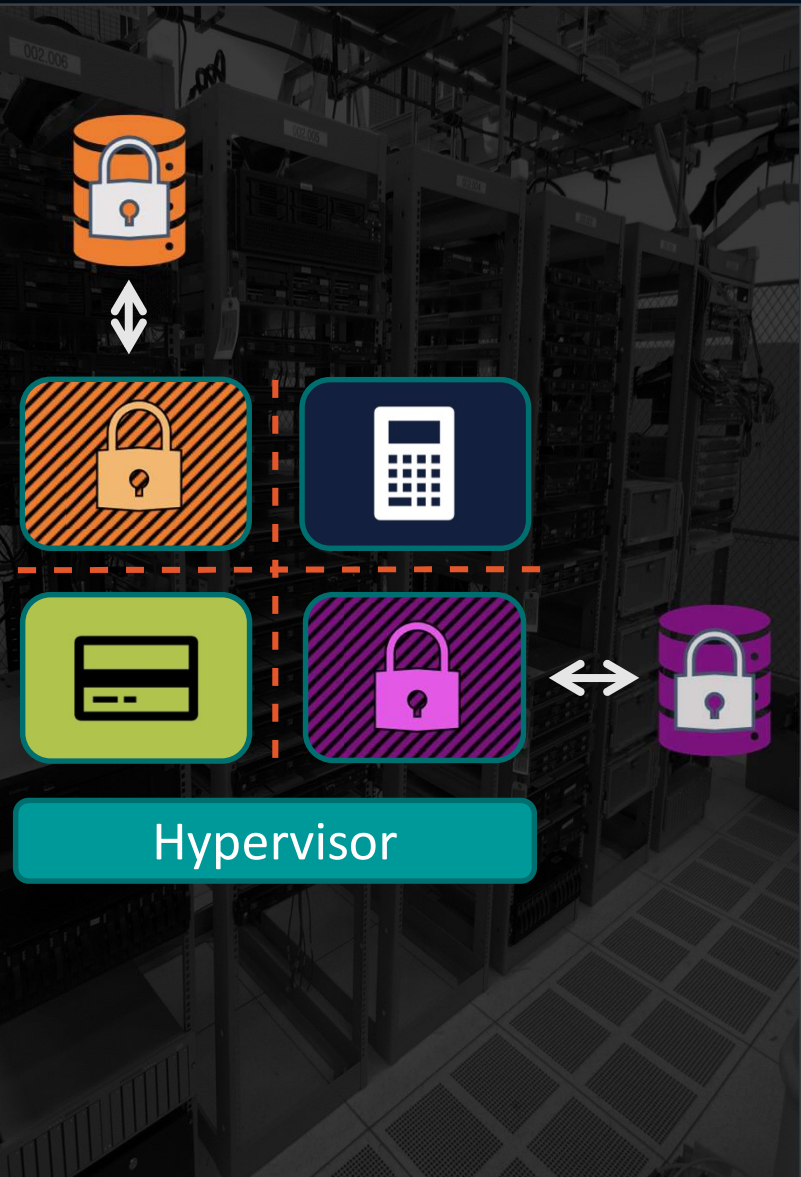
Hosts the SEV firmware that implements the SEV API

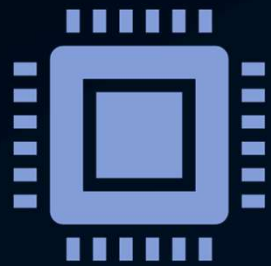
Memory encryption keys

Endorsement keys (CEK / VCEK)



AMD PSP





The AMD Secure Processor

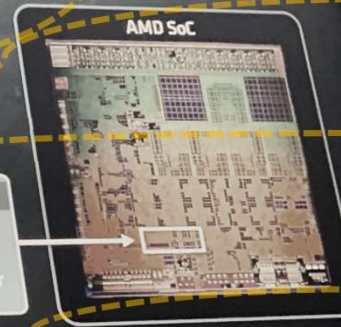
AMD SECURE PROCESSOR¹

A Dedicated Security Subsystem

- AMD Secure Processor integrated within SoC
 - 32-bit microcontroller (ARM Cortex-A5)
- Runs a secure OS/kernel
- Secure off-chip NV storage for firmware and data (i.e. SPI ROM)
- Provides cryptographic functionality for secure key generation and key management
- Enables hardware validated boot

Hardware Root of Trust Provides Foundation for Platform Security

Root of Trust
AMD Secure Processor



Server & Desktops
(Epyc & Ryzen)

integrated since 2013

undocumented,
proprietary firmware

required for **Secure Boot**

Root of trust

¹ Formerly known as *Platform Security Processor (i.e. PSP)*

Applications

SECURE ENCRYPTED VIRTUALIZATION (EPYC)

- **SEV** protects virtual machines in **untrusted** environments by encrypting VM memory
- SP manages encryption keys
- SP provides remote attestation

SECURE OS (RYZEN)

- Firmware TPM

TRUSTED EXECUTION ENVIRONMENT (RYZEN / EPYC?)

- Trusted Execution Environment
- Linux to support **SP TEE API**¹

¹ https://www.phoronix.com/scan.php?page=news_item&px=AMD-TEE-Driver-For-Linux-5.6

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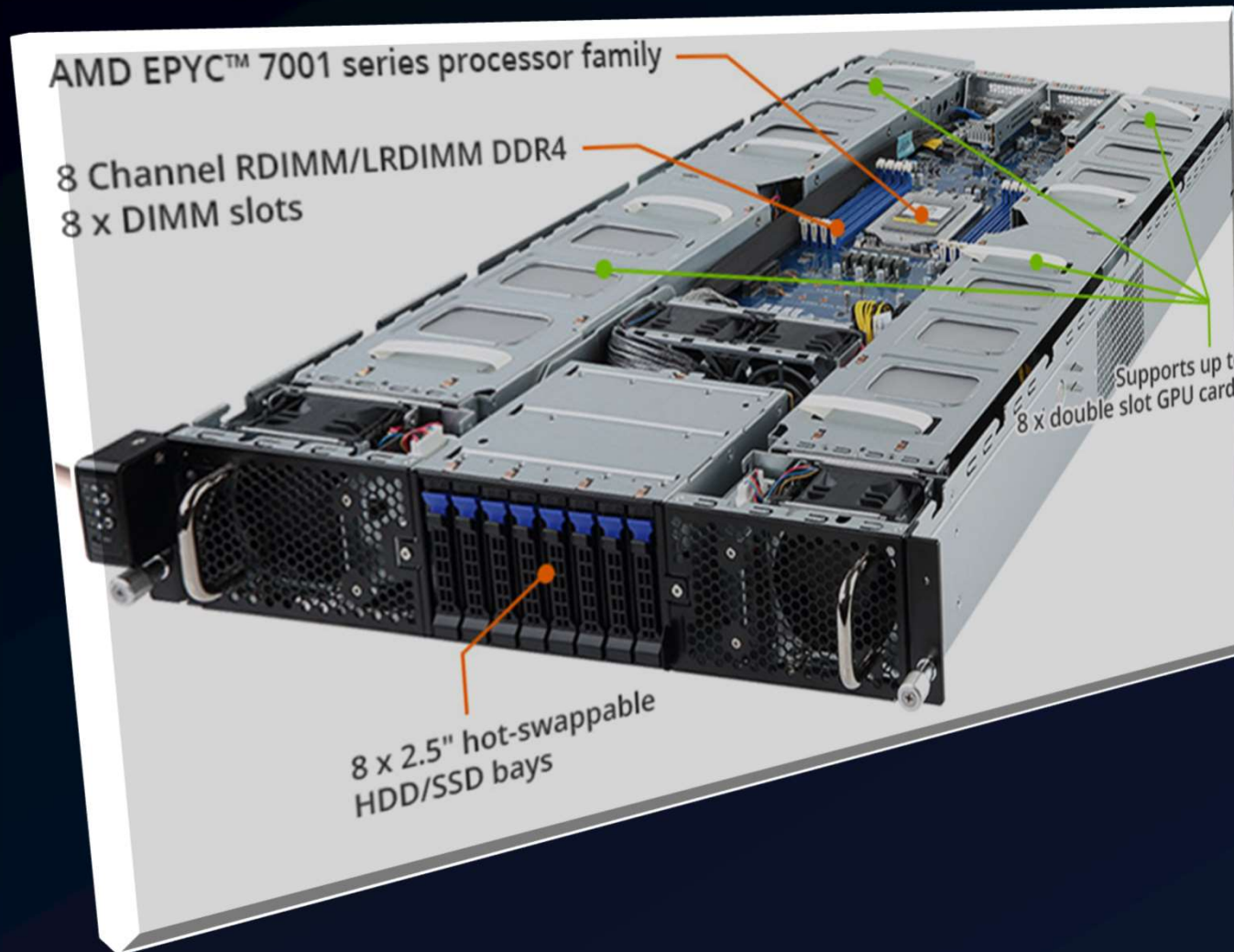
Research Question

Due to its crucial role in the SEV technology, targeting the AMD-SP instead of the protected VMs potentially allows an attacker to circumvent any protection guarantees of SEV, independent from the targeted VM!

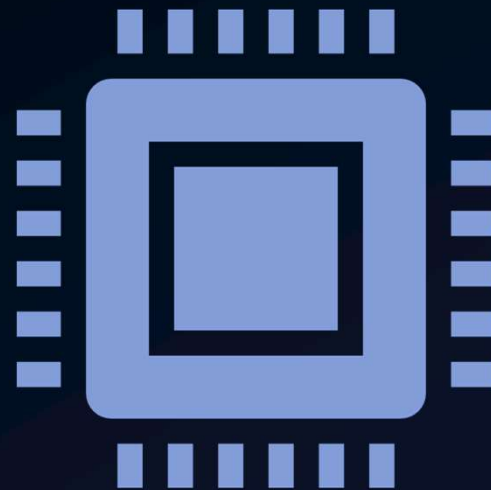
Consequently, in this work, we answer the following question:

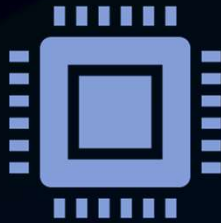
What are the implications of fault injection attacks against the AMD-SP for the SEV technology?

THE TARGET MACHINE



FIRMWARE ANALYSIS





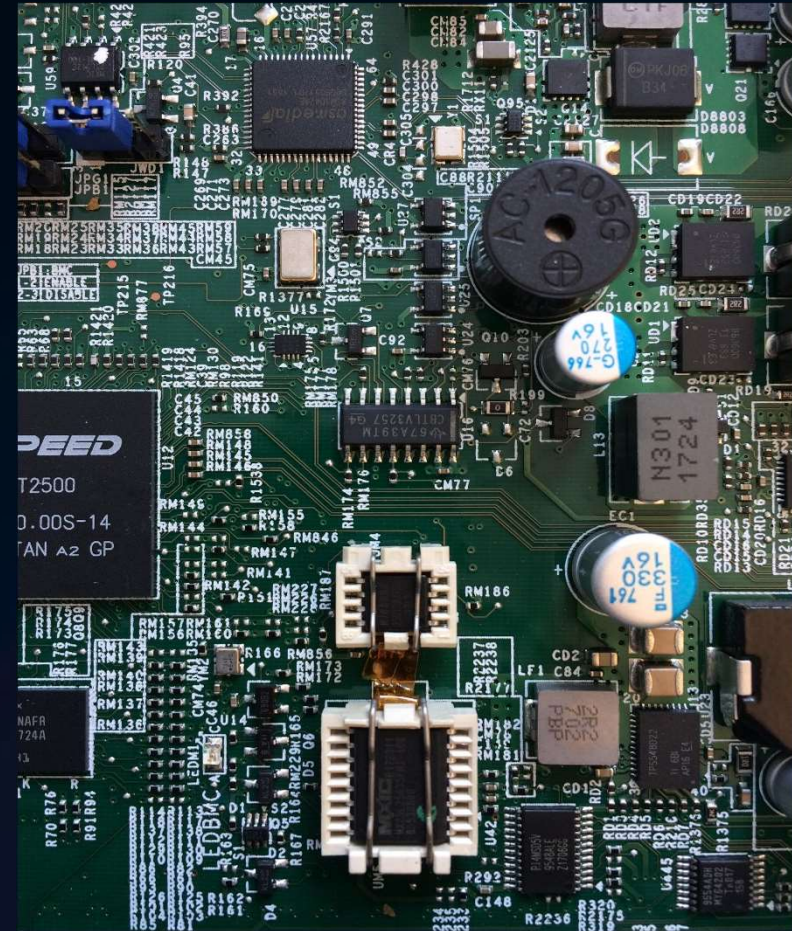
FIRMWARE ANALYSIS

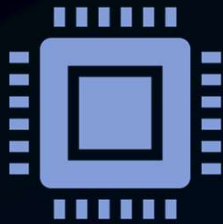
Secure Processor is part of x86 die.

- ARM Cortex A5

Firmware is stored along UEFI FW!

Updatable through UEFI update.





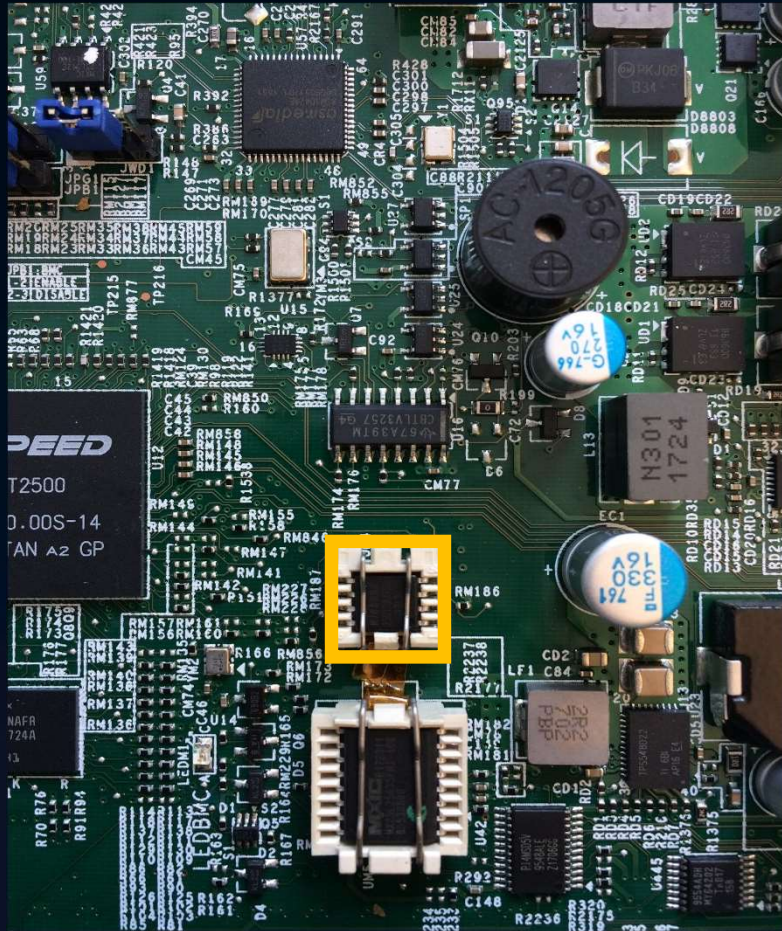
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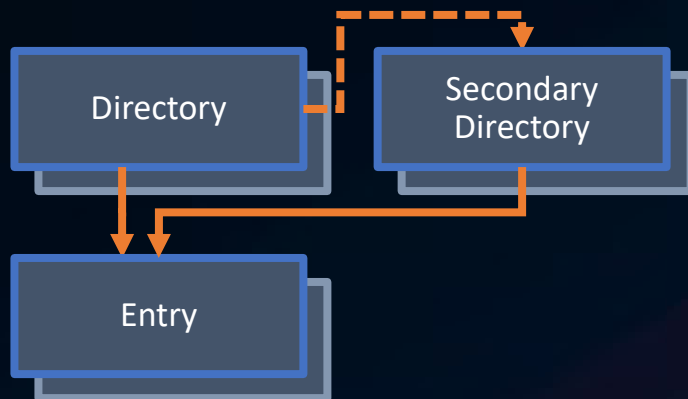
Updatable through UEFI update.



AMD SP Firmware

FIRMWARE FILE SYSTEM

- Contained within UEFI padding



```
Supermicro_H11DSU9.715
0076FD0 FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF
0076FE0 FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF
0076FF0 FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF
0077000 24 Magic50 4 Checksum 10 Count00 A004?0000
0077010 00 Type00 400 Size000 00 Address F 0000?0000
0077020 01 Type00 00000100 009414FF 00000000
0077030 03000000 80E70000 007707FF 00000000
0077040 08000000 40E10100 005F08FF 00000000
0077050 0A000000 40030000 00410AFF 00000000
0077060 12000000 40560000 00450AFF 00000000
0077070 21000000 10000000 009C0AFF 00000000
0077080 24000000 000C0000 009D0AFF 00000000
0077090 30000000 200C0000 00A90AFF 00000000
00770A0 31000000 20C00000 00B60AFF 00000000
00770B0 32000000 F0B80000 00770BFF 00000000
00770C0 33000000 70DE0000 00300CFF 00000000
00770D0 34000000 A0F10000 00F0DFF 00000000
00770E0 35000000 A0F00000 00010EFF 00000000
00770F0 36000000 40C00000 00F20EFF 00000000
0077100 40000000 Pointer to Secondary Directory 00000000
0077110 FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF
0077120 FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF
0077130 FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF
0x76FCD out of 0x1000000 bytes
```

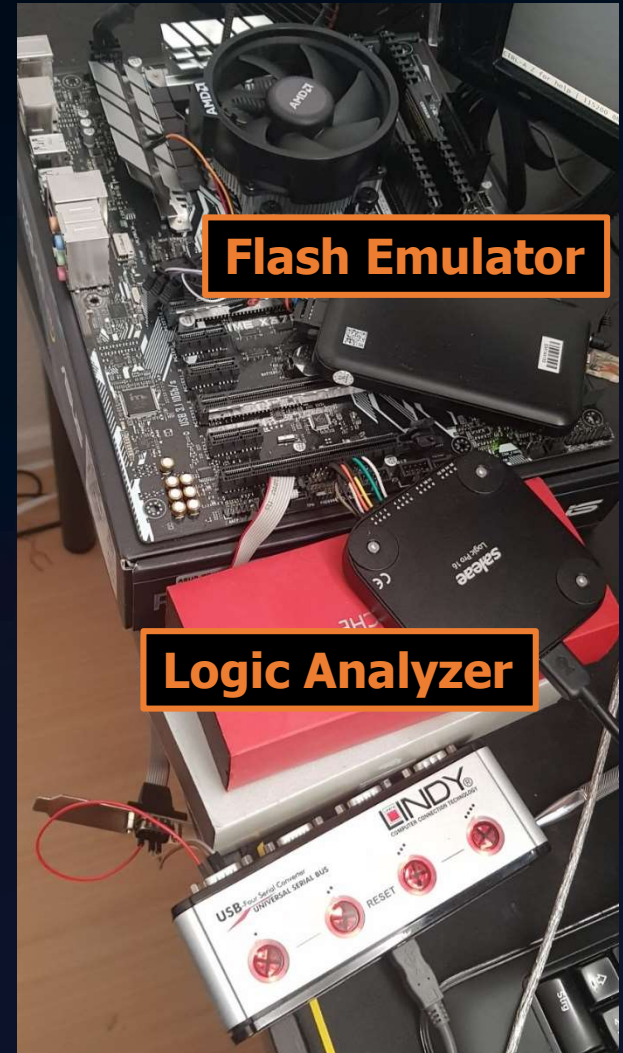
```
$ psptool uefi_image.bin
```

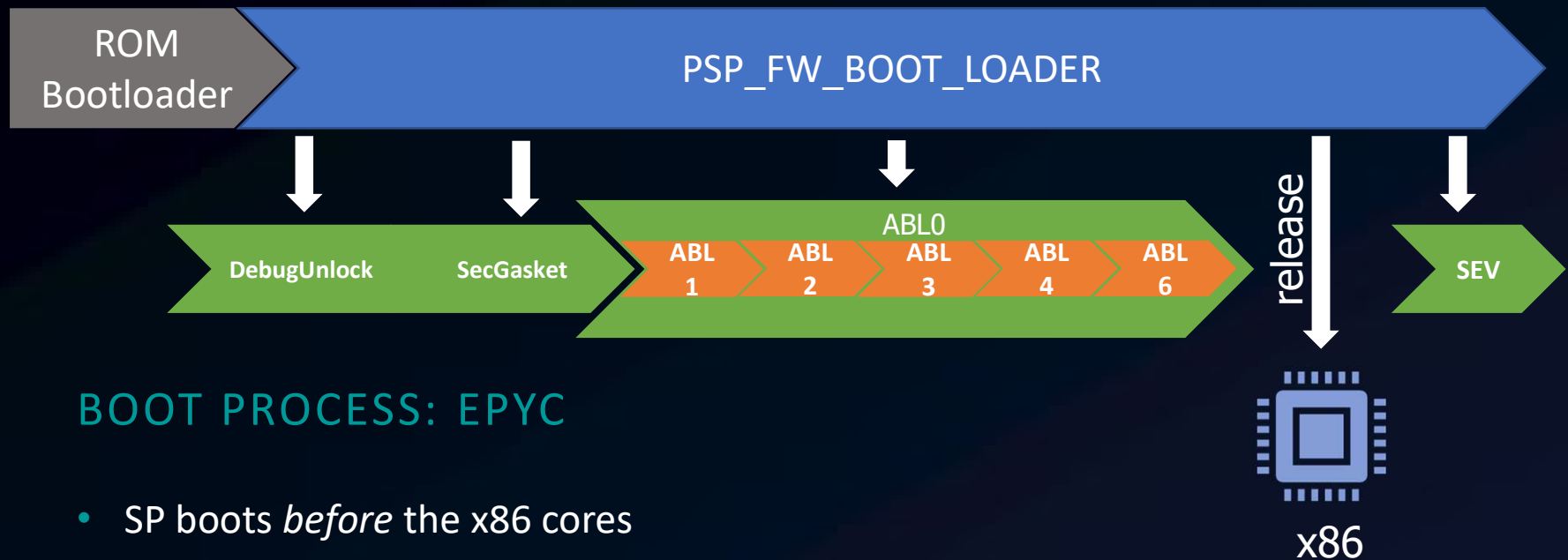
Entry	Address	Size	Type	Type Name	Version	Signed by
0	0xc2000	0x240	0x0	AMD_PUBLIC_KEY		
1	0x281000	0x8000	0x1	PSP_FW_BOOT_LOADER	0.5.0.3B	AMD_PUBLIC_KEY
2	0x289000	0x14000	0x8	SMU_OFFCHIP_FW	0.0.0.0	None
3	0xc3000	0x6000	0x3	PSP_FW_RECOVERY_BOOT_LOADER	0.5.0.17	AMD_PUBLIC_KEY
4	0xc9000	0x340	0x5	BIOS_PUBLIC_KEY		
5	0xffff000	0x1000	0x6	BIOS_RTM_FIRMWARE		
6	0x29d000	0x1e000	0x2	PSP_FW_TRUSTED_OS	0.5.0.3B	AMD_PUBLIC_KEY
7	0xa0000	0x10000	0x4	PSP_NV_DATA		
8	0x2bb000	0x14000	0x108	PSP_SMU_FN_FIRMWARE	0.0.0.0	None
9	0xca000	0x340	0x9	AMD_SEC_DBG_PUBLIC_KEY		
10	0x1	0xffffffff	0xb	AMD_SOFT_FUSE_CHAIN_01	E9.0.0.0	None
11	0xcb000	0x340	0xd	PSP_BOOT_TIME_TRUSTLETS_KEY		

psptool: <https://github.com/PSPReverse/psptool>

psptrace: <https://github.com/PSPReverse/PSPTool>

No.	Address	Size	Type	Info
0	0xfa0000	0x18	!UEFI-IMAGE	[c]
3	0xc20000	0x10	Unknown area	[c]
5	0x020000	0x32	Firmware Entry Table	
6	0x0c0000	0x6a	Unknown area	CCP [c]
8	0x2a9000	0xfc	Directory: \$PSP	CCP [c]
12	0x2a9400	0x440	AMD_PUBLIC_KEY	CCP [c]
			~ 60 μ s delay ~	
29	0x798400	0xd0c0	PSP_FW_BOOT_LOADER	CCP [c]
			~ 2025 μ s delay ~	
864	0x798000	0x100	!PL2_SECONDARY_DIRECTORY	CCP [c]





BOOT PROCESS: EPYC

- SP boots *before* the x86 cores
- **On-Chip** Bootloader loads **Off-Chip** bootloader from flash
- **Off-Chip** Bootloader loads and executes apps in specific order
- System is initialized by different **ABL stages**
- Load UEFI image and release x86 cores from reset
- **SEV app** is loaded during runtime upon the **request of the OS**

Agenda

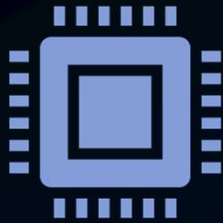
Amusing history

What is Zen/AMD SEV?

Research question

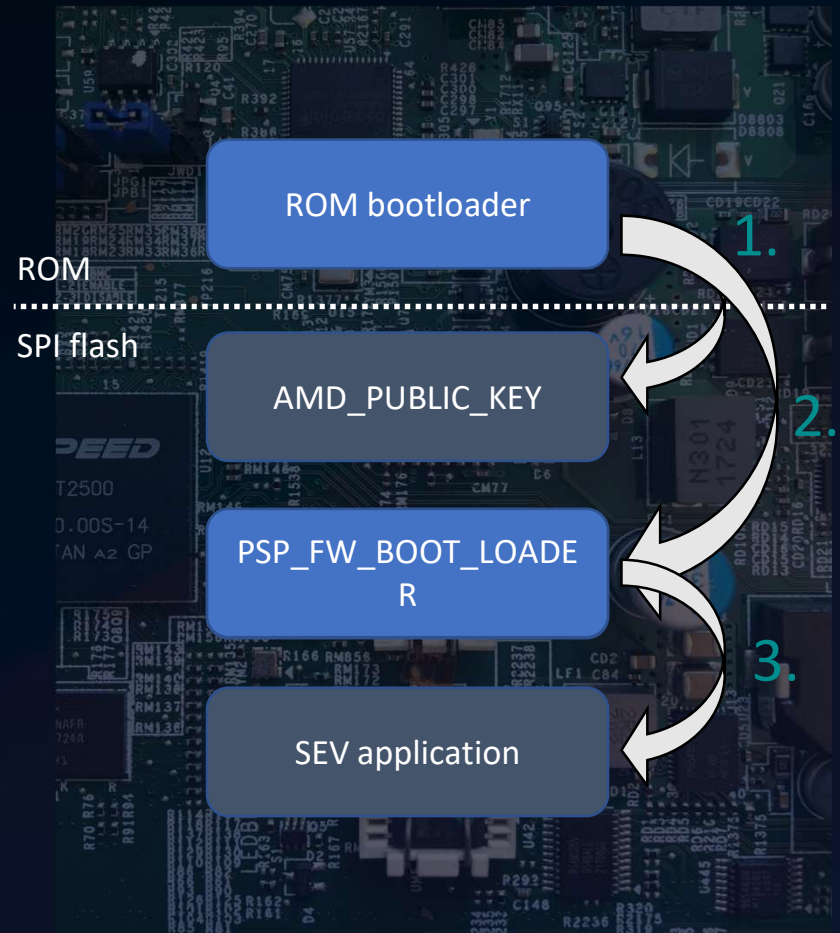
Glitching the AMD SP

Conclusions



FIRMWARE ANALYSIS

1. Load & verify AMD_PUBLIC_KEY
 - verify using hash
2. Load & verify PSP_FW_BOOT_LOADER
 - verify using public key
3. Load & verify SEV application
 - verify using public key



ROM
Bootloader

PSP_FW_BOOT_LOADER

No.	Address	Size	Type	Info
0	0xfa0000	0x18	!UEFI-IMAGE	[c]
3	0xc20000	0x10	Unknown area	[c]
5	0x020000	0x32	Firmware Entry Table	
6	0x0c0000	0x6a	Unknown area	CCP [c]
8	0x2a9000	0xfc	Directory: \$PSP	CCP [c]
12	0x2a9400	0x440	AMD_PUBLIC_KEY	CCP [c]
			~ 60 μ s delay ~	
29	0x798400	0xd0c0	PSP_FW_BOOT_LOADER	CCP [c]
			~ 2025 μ s delay ~	

864	0x798000	0x100	!PL2_SECONDARY_DIRECTORY	CCP [c]
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...

EXPERIMENTING A BIT ...

No.	Address	Size	Type	Info
0	0xfa0000	0x18	!UEFI-IMAGE	[c]
3	0xc20000	0x10	Unknown area	[c]
5	0x020000	0x32	Firmware Entry Table	
6	0x0c0000	0x6a	Unknown area	CCP [c]
8	0x2a9000	0xfc	Directory: \$BSP	CCP [c]
12	0x2a9400	0x440	AMD_PUBLIC_KEY	CCP [c]

Constant # of level changes

Continued SPI activity

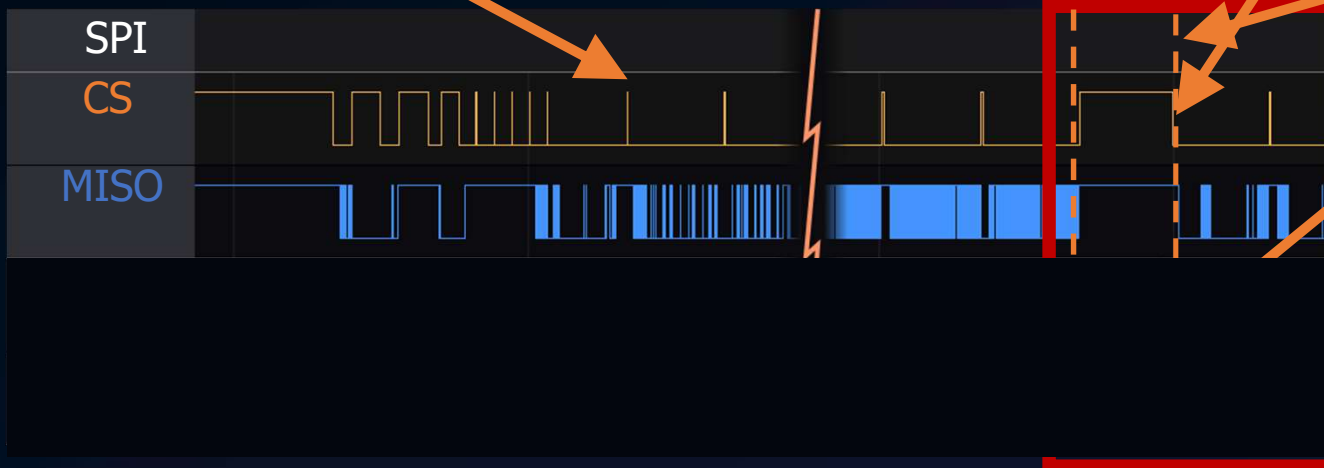
Key verification!

-> glitch "window"

No SPI activity

Original pubkey

Modified pubkey



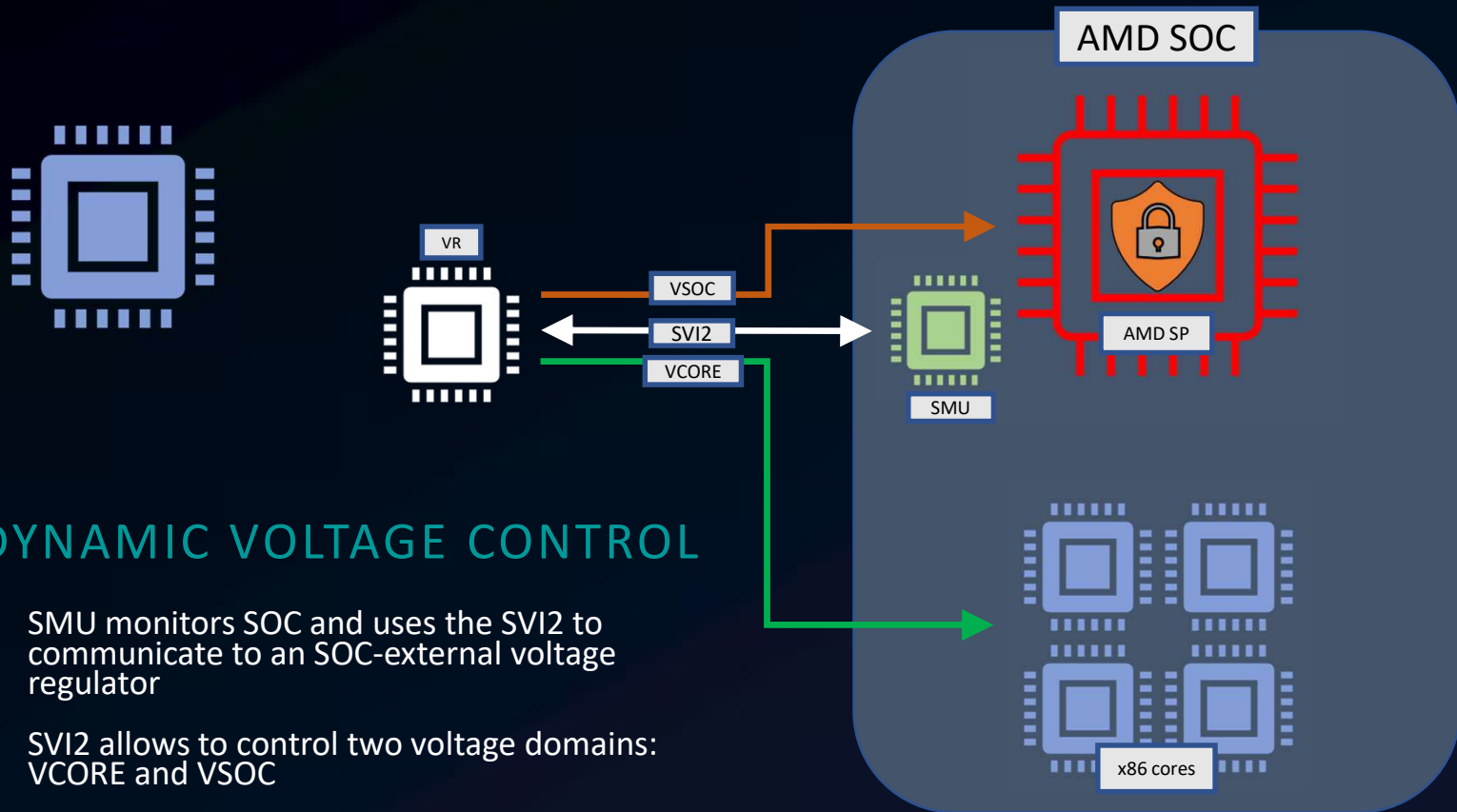
ATTACK OVERVIEW

Our goal is to execute our own payload right after the ROM bootloader.

1. Create custom public key
2. Replace AMD_PUBLIC_KEY in UEFI image
3. Replace PSP_FW_BOOT_LOADER component with payload
4. Sign payload with custom key
5. Glitch pubkey verification

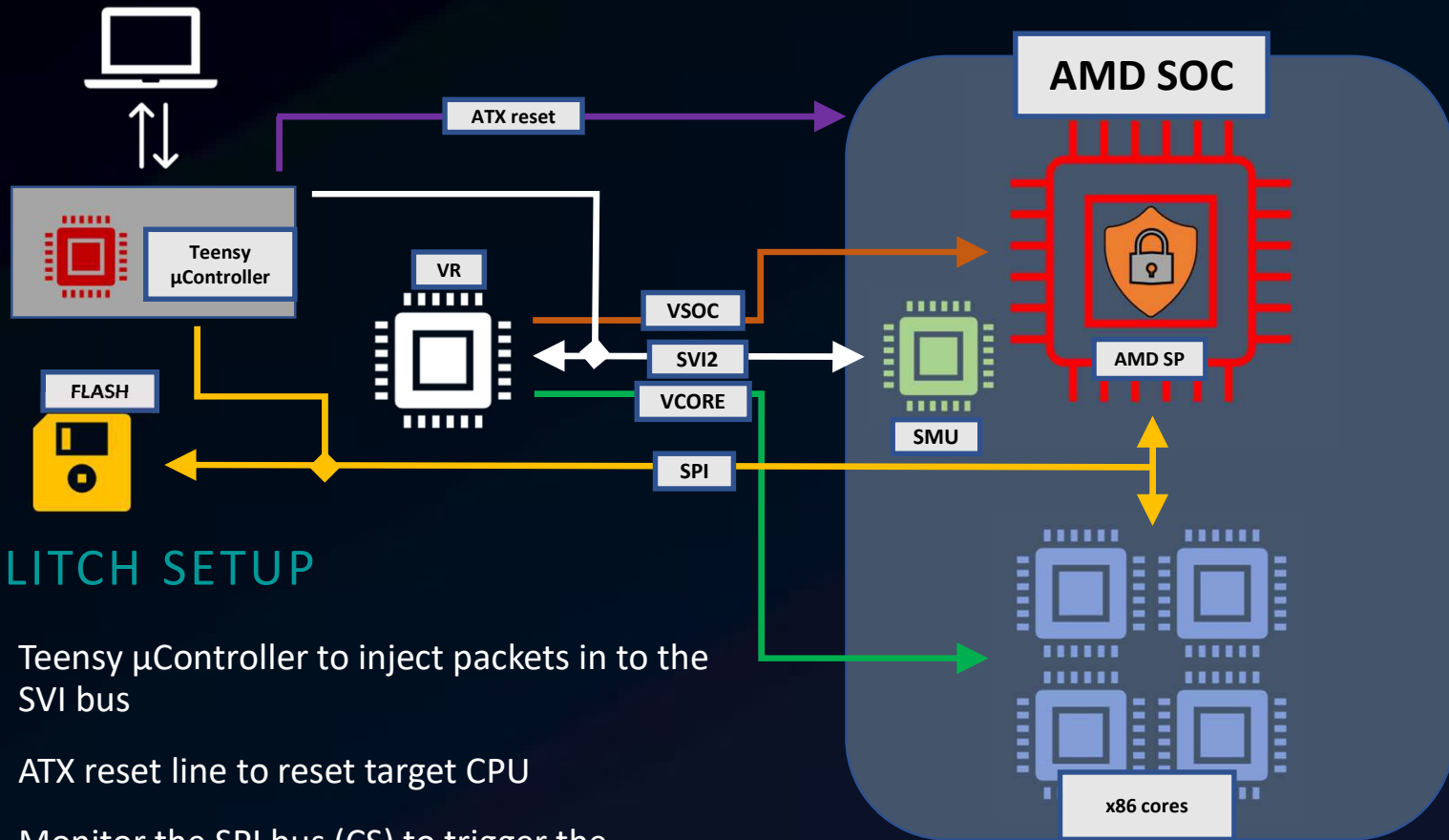
No.	Address	Size	Type	Info
0	0xfa0000	0x18	!UEFI-IMAGE	[c]
3	0xc20000	0x10	Unknown area	[c]
5	0x020000	0x32	Firmware Entry Table	
6	0x0c0000	0x6a	Unknown area	CCP [c]
8	0x2a9000	0xfc	Directory: \$PSP	CCP [c]
12	0x2a9400	0x440	CUSTOM KEY	CCP [c]
			~ 60 μ s delay ~	
29	0x798400	0xd0c0	PAYLOAD	CCP [c]
			~ 2025 μ s delay ~	
864	0x798000	0x100	!PL2_SECONDARY_DIRECTORY	CCP [c]





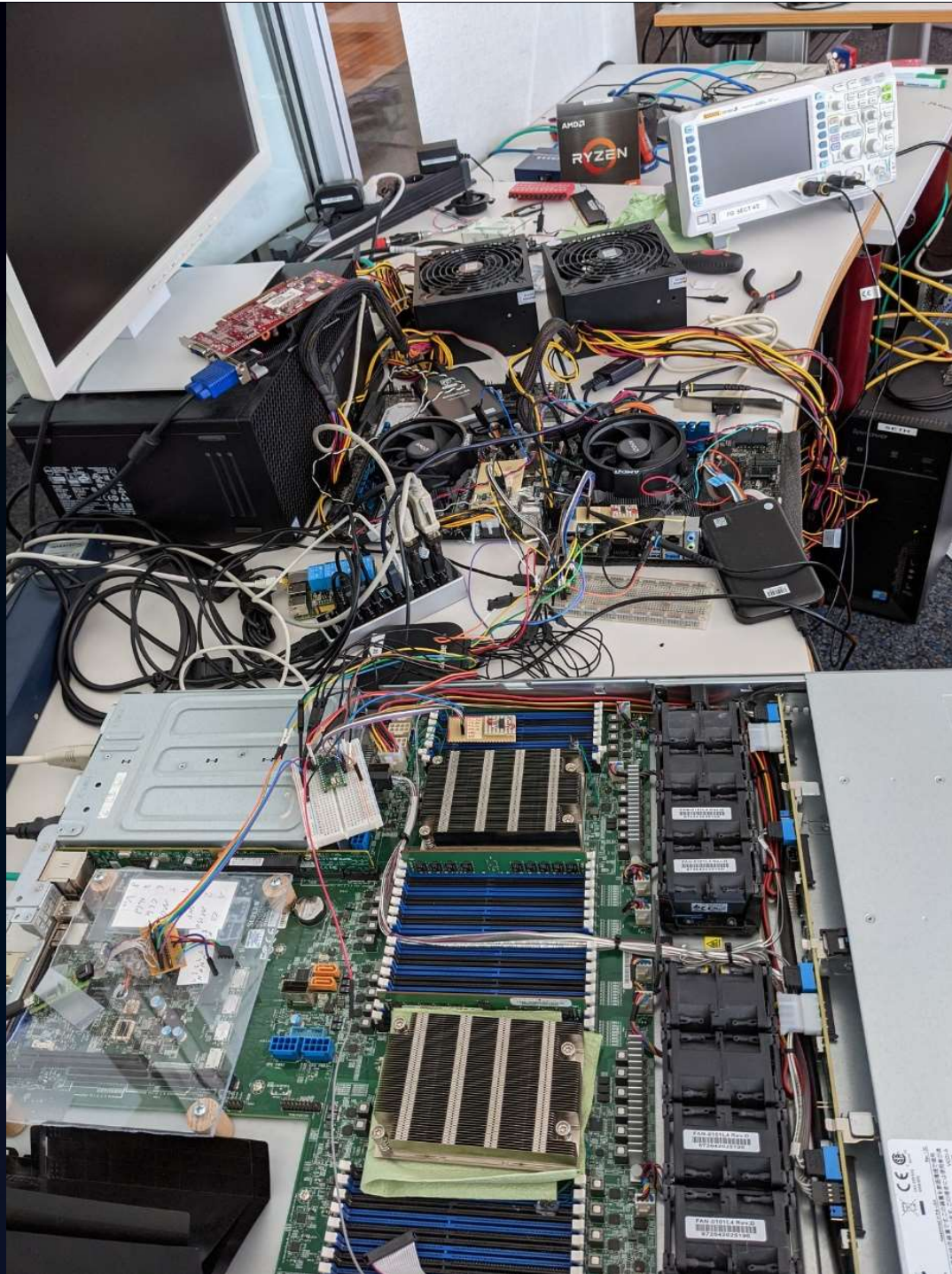
DYNAMIC VOLTAGE CONTROL

- SMU monitors SOC and uses the SVI2 to communicate to an SOC-external voltage regulator
- SVI2 allows to control two voltage domains: VCORE and VSOC
- Ryzen: AMD-SP uses VSOC
- Epyc: AMD-SP uses VCORE of a dedicated VR (two VRs per CPU)



GLITCH SETUP

- Teensy μ Controller to inject packets in to the SVI bus
- ATX reset line to reset target CPU
- Monitor the SPI bus (CS) to trigger the voltage glitch
- Control glitch parameters via external PC

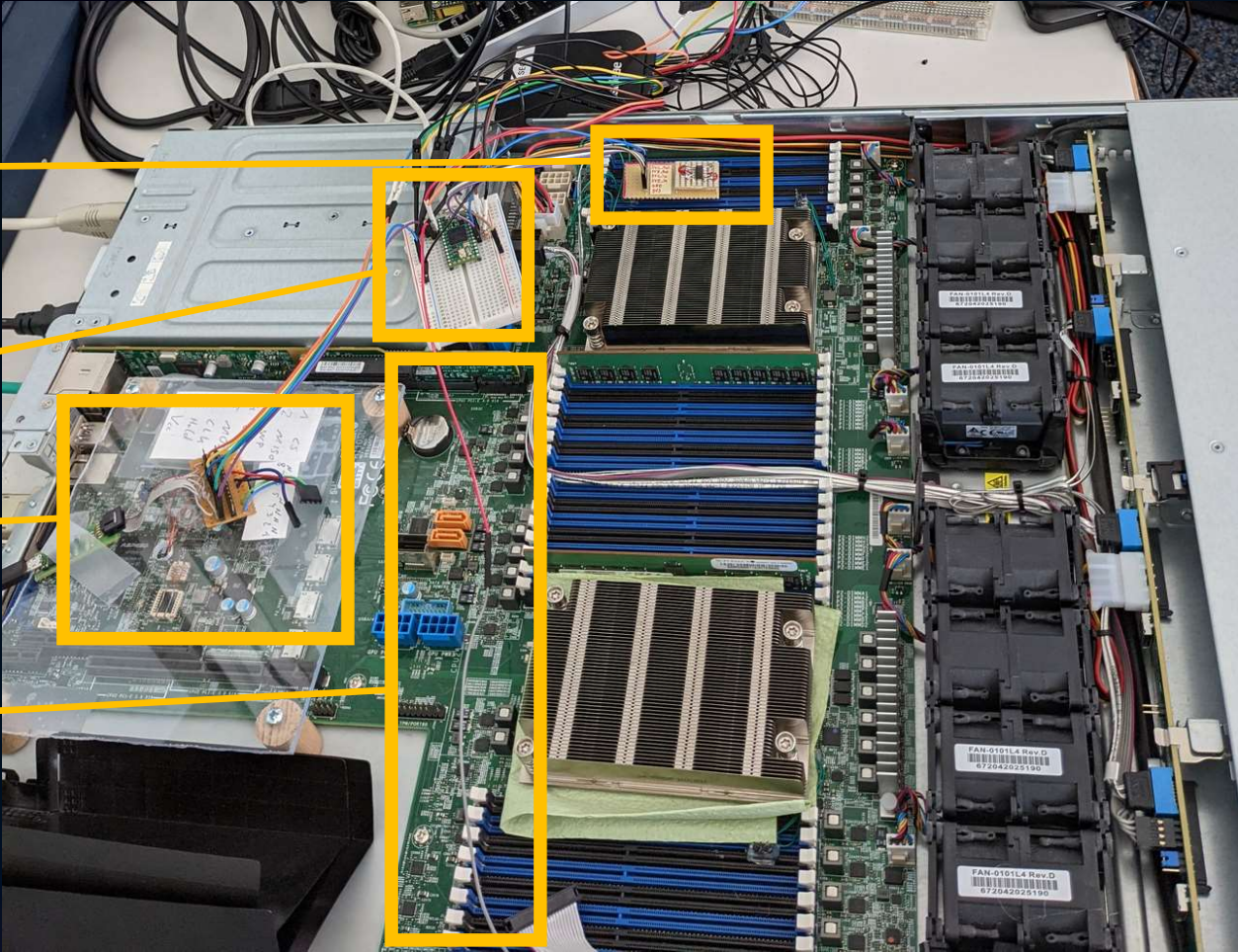


SVI2 access

Teensy
 μ Controller

SPI access

ATX reset

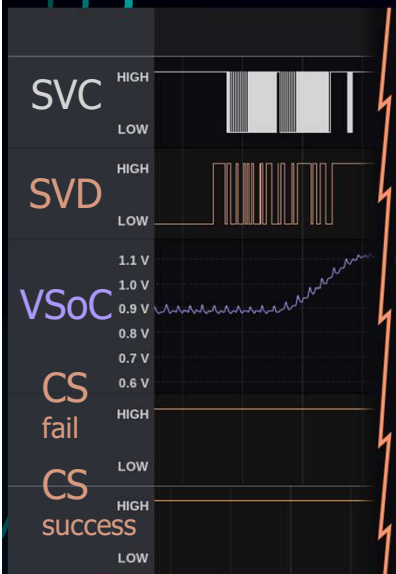


Glitch steps



- SVI2 SVC – clock, CPU/VR (shared)
- SVI2 SVD – data from CPU, pulled low when inactive
- VSoC – target input voltage
- SPI CS – SPI's chip-select signal (successful/failed pubkey verification)

Glitch steps



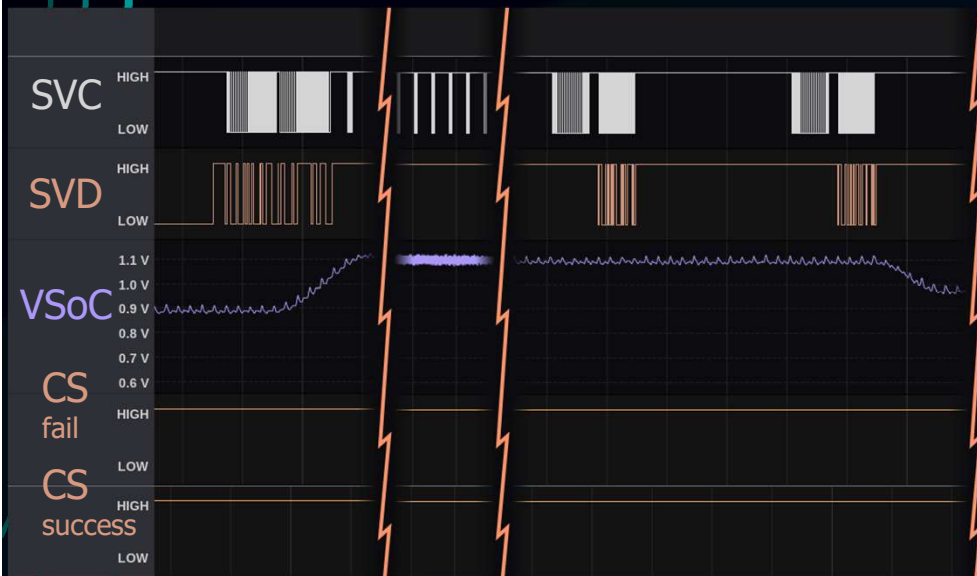
- SVI2 SVD: becomes high -> start attack logic
- CPU initially configures voltage

Glitch steps



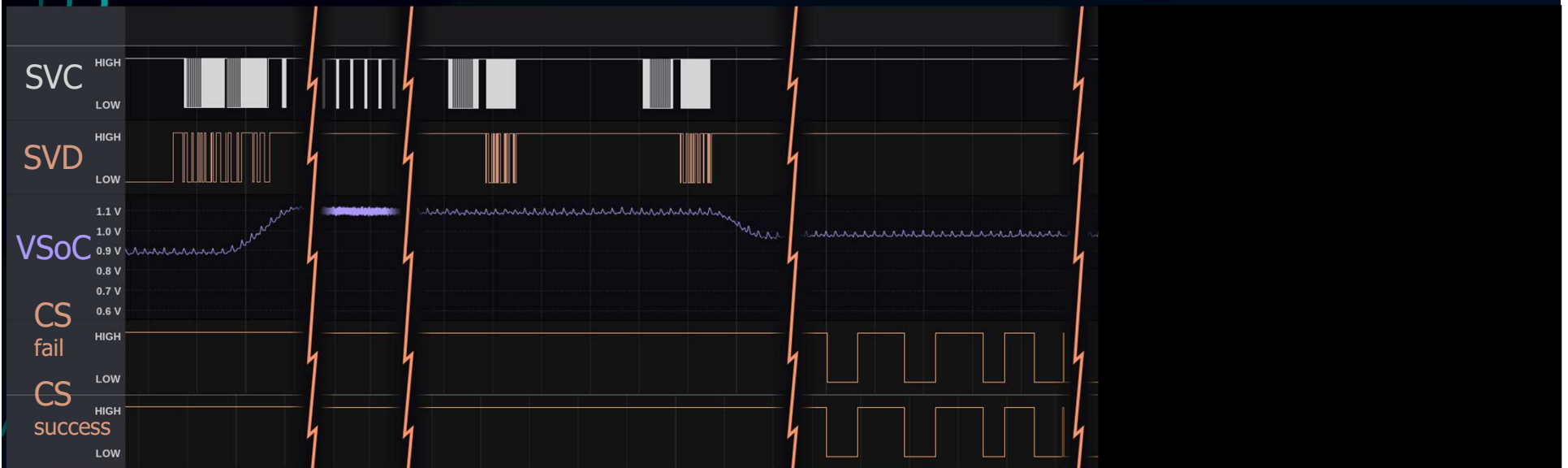
- SVI2 SVD: becomes high -> start attack logic
- CPU initially configures voltage
- VR constantly sends telemetry data to CPU

Glitch steps



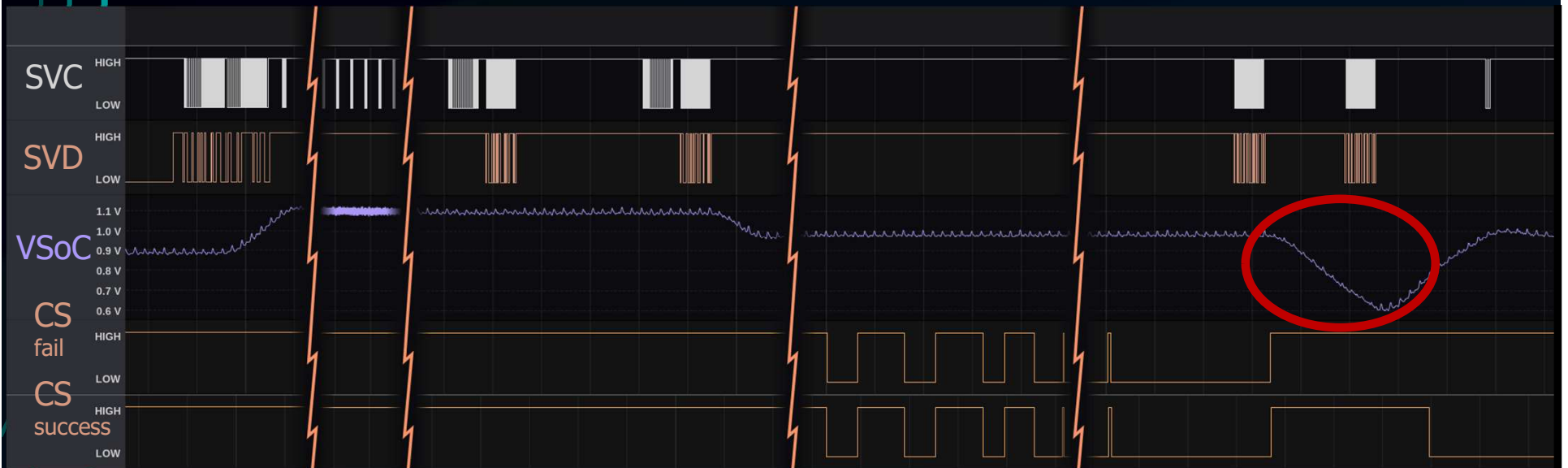
- SVI2 SVD: becomes high -> start attack logic
- CPU initially configures voltage
- VR constantly sends telemetry data to CPU
- Inject packets to disable telemetry -> avoids packet collision

Glitch steps



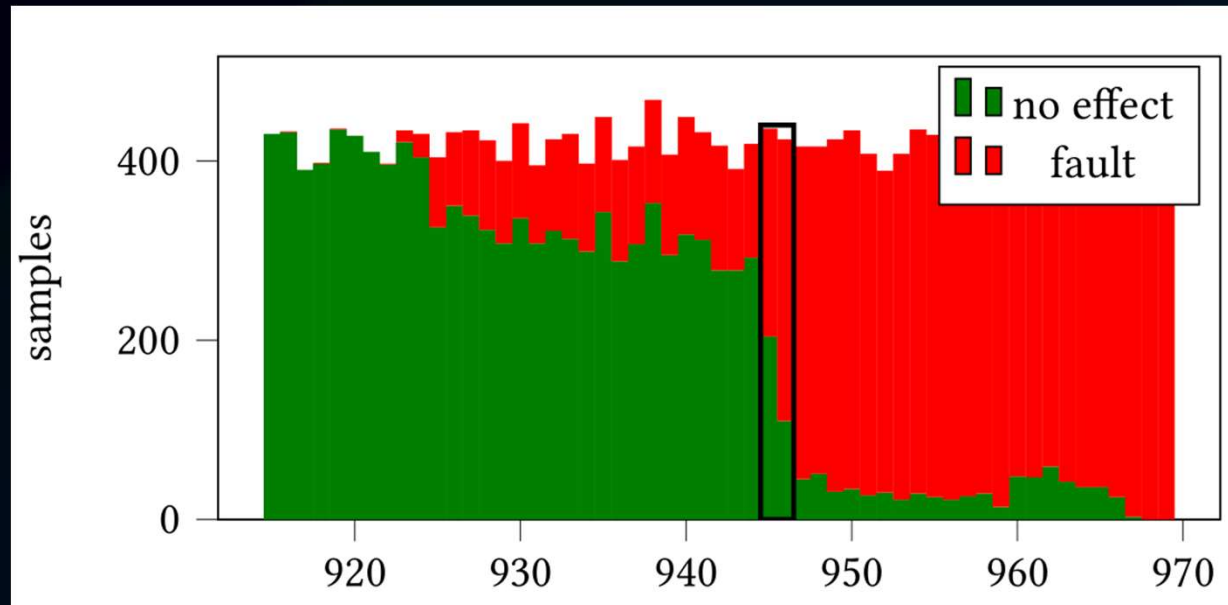
- Wait until SPI CS becomes active

Glitch steps

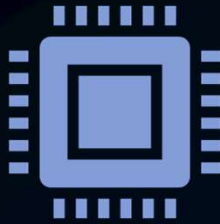


- Wait until SPI CS becomes active
- Count # of CS level changes to time glitch
- Inject packet to drop voltage and to revert to the original voltage level
- Verify success by observing CS again -> reset if CS not "low" after timeout
- Glitch duration window size

Duration window



- SPI image with original AMD public key
- Glitch introduced during the “glitch window”
- no effect: AMD-SP continued to boot -> CS is low after the “glitch window”
- fault: AMD-SP failed to boot -> CS is high after the “glitch window”

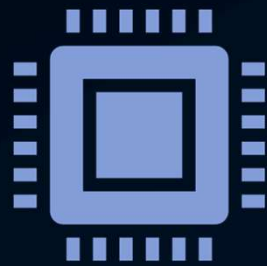


RESULTS

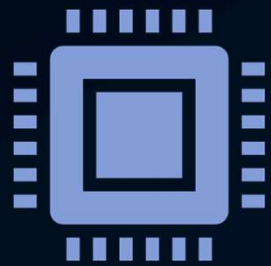
- Epyc and Ryzen CPUs are affected
- Successful glitch between every ~13min (Zen 1) and every ~46min (Zen 3)

Payloads:

- SPI “Hello World”
- Decrypt firmware (Zen 3)
- Dump ROM bootloader to SPI bus
- SEV-policy override (Zen 2):
 - Boot system with patched SEV firmware: Enables the “DBG_DECRPYT” SEV API command regardless of a guest’s SEV policy
- Dump (V)CEK secrets to the SPI bus



Reverse-engineering SEV's (V)CEK key derivation



Attacks

Attacker types



Malicious cloud administrator:

- Full hypervisor access
 - Send commands to the AMD-SP: SEV API
- Cloud management access
 - Able to install new systems in the datacenter
 - Able to migrate a VM to a different system



Malicious tenant + VM escape:

- Full hypervisor access
 - Send commands to the AMD-SP: SEV API

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RESOURCES

<https://github.com/RobertBuhren/amd-sev-migration-attack>

- Proof-of-concept implementation of the migration attack.

<https://github.com/RobertBuhren/Insecure-Until-Proven-Updated-Analyzing-AMD-SEV-s-Remote-Attestation>

- Proof-of-concept signature created with an extracted CEK.

<https://github.com/PSPReverse/PSPTool>

- psptool & psptrace

<https://lsseu2019.sched.com/event/TynP/upcoming-x86-technologies-for-malicious-hypervisor-protection-david-kaplan-amd>

- AMD SEV-SNP Talk at the Linux Security Summit 2019.

One Glitch to Rule Them All: Fault Injection Attacks Against AMD's Secure Encrypted Virtualization,
R. Buhren, H. N. Jacob, T. Krachenfels, J.-P. Seifert, ACM CCS 2021.

Insecure Until Proven Updated: Analyzing AMD SEV's Remote Attestation,
R. Buhren, J.-P. Seifert, Christian Werling, ACM CCS 2019.



Thank you for your attention!

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Questions?

